Independent Transmitter Monitor Design Details

Index | Page

1.0 Introduction

A survey of the schemes published on the internet and in the RADCOM magazine carried out by the North Cheshire Radio Club showed that there were various techniques available for remote operation via the internet but none of them appeared to properly address any/all of the safety related issues for truly remote operation.

The UK Ofcom terms and conditions (Ref.1) include the requirement that any communication links used to control the Radio Equipment are failsafe such that any failure will not result in unintended transmissions or any transmissions of a type not permitted by the Licence.

A failsafe or fail-secure device is one that, in the event of a specific type of failure, responds in a way that causes no harm, or at least minimum harm to other devices or personnel. Zero risks can never be achieved, but non-tolerable risks must be reduced 'As low As Reasonably Possible' (ALARP). Fortunately detailed guidance on the design procedures for safety related systems is given in IEC 61508 parts 1 to 7, with part 1 covering the general requirements (Ref.2)

The design process therefore began with a description of the 'Overall Scope', followed by a 'Hazard and Risk Analysis', leading to the 'Overall Safety Requirements', using the Radio Club's Kenwood TS-480HX 200Watt hf transceiver as a concrete example. This was reported in the hazop.pdf document which can be downloaded from the web page on 'Remote Transmitter Operation' given in Ref. 3. A key part of this study identified that the current methods of remote operation (2015) could be made sufficiently failsafe as required by Ofcom by having an independent transmitter monitor system built in accordance with IEC61508.

2.0 Basic Specification of the Independent Transmitter Monitoring System

Its functions are:-

- To trip and turn off the power to the transmitter if it transmits continuously for more than 4 minutes.
- To trip and remove the power from the transmitter equipment and control system if the temperature of the cubicle walls reach 40ºC.
- To trip if the mains supply is interrupted.
- To require a manual reset if tripped.

It was judged that the 'failure modes' leading to 'uncontrolled transmissions' and to 'over temperature' were 'critical' and hence their likelihoods needed to be made 'remote'. This meant that their wrong side failure rates should not be more than once in 10E5 years (i.e. 1000 000 000 hours).

Note: The transmitter would normally have its 'time-out time' set to 3 minutes to avoid invoking this 'transmitter monitor shut down system'. However the transmitter relies on complex software and the time out feature is not claimed to be failsafe. Hence the need for a shut-down system with sufficient in-built redundancy to achieve the very low wrong side failure rate required for the safety related function of ensuring the transmitter can be turned off remotely.

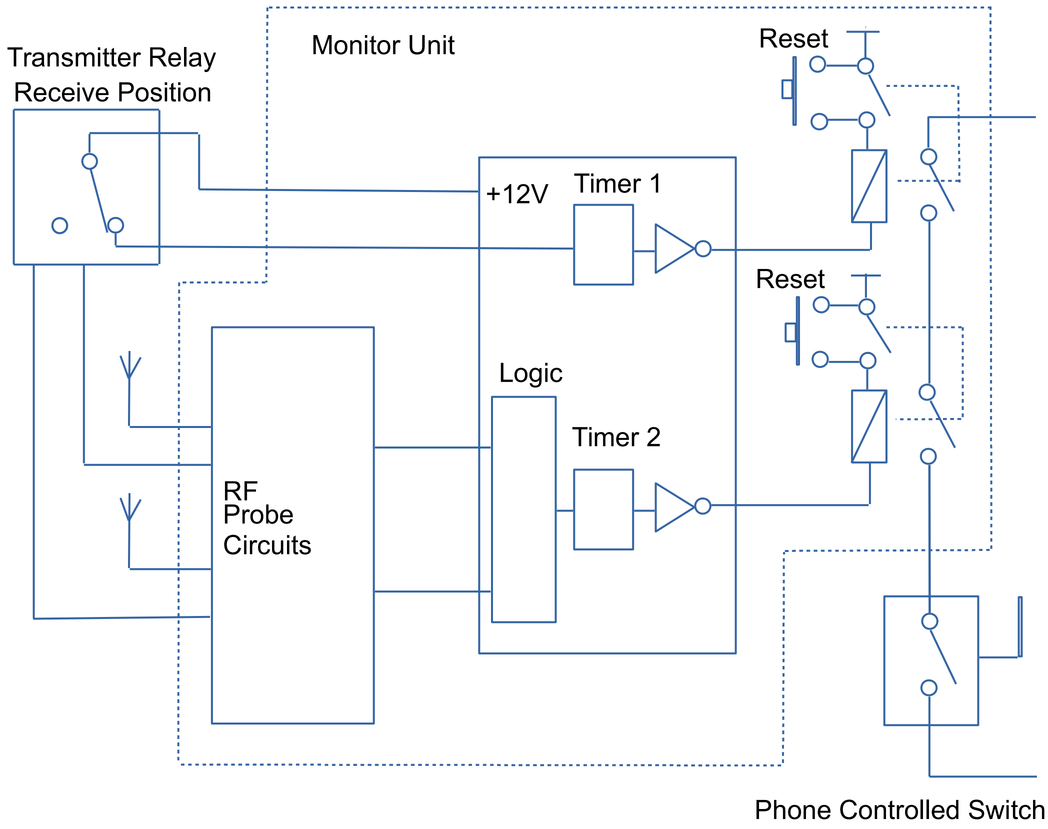
It is shown in section 17 of Ref.3 that the reliability of the transmitter monitor shut down system could be achieved with a triple redundant design.

- The first subsystem is a power switch controlled via a mobile phone. The failure rate is dominated by the drop out rate of the mobile phone messaging system. It has been shown in section 17-B1 (Ref.3) that the network can be prescribed to have a reliability of 0.99 (Note: '0' means zero reliability and '1' means perfect reliability).
- The second subsystem is a relay in a latching circuit which has a time out circuit reset via a contact on the transmitter power amplifier control relay. A manually operated push button is used to set the circuit. The arrangement is to be designed to have a wrong side failure rate of not more than 0.000 01 failures per hour.
- The third sub system is another relay in a latching circuit which has a time out circuit reset via another circuit which detects the absence of RF power in the feeder. A manually operated push button is used to set the circuit. The arrangement is to be designed to have a wrong side failure rate of not more than 0.000 01 failures per hour.
- Two thermostatic switches designed to trip at 40ºC are to be used to monitor the temperature of the cabinet walls. They are to be be wired in series and arranged to interrupt the mains supply and thus trip the two relays used in the time out circuits. It is shown in section 17-B2 (Ref.3) that this configuration can achieve the required reliability.

3.0 Transmitter Monitor Unit Design Description

The basic block schematic is shown in Fig.1. It features two independent time out circuits (Timer-1 and Timer-2) which are reset when the transceiver returns to the receiving mode.

Fig.1 : Independent Transmitter Monitoring System – Basic Block Schematic



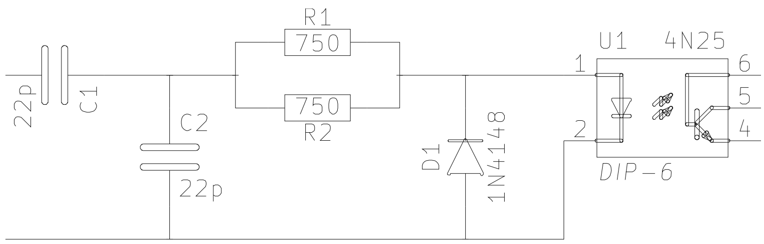
3.1 Transmitter Relay Circuit

Timer-1 is reset by a 12V signal received via the relay within the transceiver used to operate the antenna relay in an external linear amplifier if present. In the case of the TS-480HX transceiver an internal signal labelled TSB is generated internally which is OV when receiving and 7.5V when in the transmitting mode. Amongst other things, this signal is used to drive a transistor to power the antenna relay for the TS-480HX, and another transistor to energise the relay included to operate the linear amplifier antenna relay. The reliability of this second relay is dominated by the integrity of the TSB signal. If it stays permanently low then the first relay stays in the receiving mode so that the transmitter output stage is not connected to the antennas and no signal gets out anyway. The wiring between the transceiver relay and the Timer board is arranged so that any disconnection results in the loss of the reset signal and the Timer-1 times out and trips the power. The signal is interfaced to the timer board via an opto-isolator.

3.2 RF Probe Circuits

Timer-2 is reset by the absence of any detectable RF output to the antennas. The TS-480HX transceiver can be switched between two antenna outputs. The voltages on the two co-axial feeders are therefore detected by two independent RF probe type circuits of the form shown in Fig.2, and the counter is reset by the absence of RF on which ever antenna happens to be in use. Each probe is rated to detect RF power from 4 to 400 Watts into a nominal 50 Ω antenna impedance, over the frequency range 1MHz to 30MHz. The probe circuits use a capacitive divider to reduce the power loss in the resistors which limit the current in the diodes. A 3.68MHz oscillator is provided to facilitate the testing of the probes and the Timer-2 circuit. Two relays are used to switch the probe circuit between the antenna input and the test signal. The relays are wired so that a failure to operate is either detected by the lack of a test signal during testing, or by the loss of the transmitter output connection to the antenna. The probe circuits and the testing circuit are housed together in their own aluminium enclosure to help screen the RF from the rest of the monitor circuit.

Fig.2 RF Probe Circuit



3.3 Timer Board

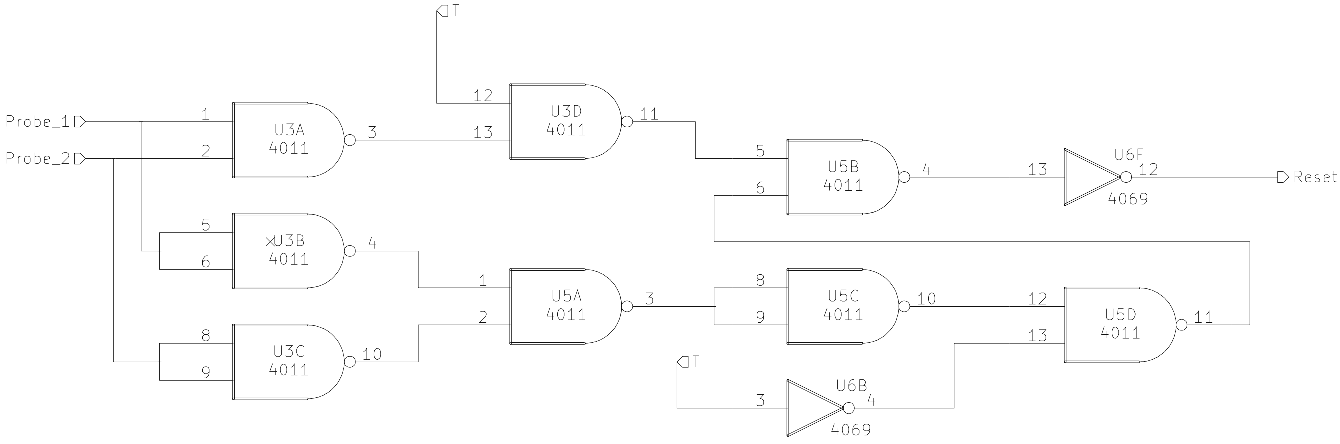
The two timer circuits are independent of each other for redundancy purposes.

Timer-1 is based on the cmos CD4060 14-stage ripple counter. It is held in the reset condition which forces all the outputs to be zero when the transmitter is in the receiving mode. It will time-out by counting up to 16384 pulses (2^{14}) whereupon the chosen output goes high and de-energises the relay to stop the transmission. The frequency of the pulses are determined by two resistors and a capacitor in associating with an oscillator circuit made up from two inverters within the chip.

Timer-2 is based on the cmos CD4020 14-stage ripple counter which is similar in function to the CD4060 chip but does not contain the inbuilt oscillator stage. The oscillator is therefore constructed using two inverter stages of a CD4069 Hex inverter. The CD4020 is used instead of another CD4060 chip to avoid common mode failures in these key items. The oscillator components are chosen to give a time out period of approximately 3.5 minutes so that they fall comfortably between the 3 minutes of the transmitter time-out setting and the 4 minutes chosen for the backstop. This avoids the need for select-on-test components.

The Logic stage (Fig.3) interfacing the probe signals to the second timer has been added to simplify the testing. In normal operation whichever of the two probe circuits that is in use can control the timer. However when in the testing mode (i.e. T=L) both probe signals have to be present to allow the counter to time out. The test is invoked by switching 12V onto the test relays and the 3.68MHz oscillator to activate the probe circuits. This also switches the logic circuit into the test mode via a transistor interface to the 9V timer board which produces the 'T' signal for the logic.

Fig.3 Timer Board Logic Circuit



Note: #1 Absence of RF results in the probe signal being High at the timer board.
#2 When T = H the output of U3D is forced high.
#3 When T = L the output of U5D is forced high.

The required Truth Tables are:-

When T = H (Normal Mode)

Table 1

Probe_1	Probe_2	Output
H	H	H
L	H	L
H	L	L
L	L	L

When T = L (Testing Mode)

Table 2

Probe_1	Probe_2	Output
H	H	H
L	H	H
H	L	H
L	L	L

Table 3 : Logic Truth Table – Normal Operation

T	P1	P2	3A	3B	3D	5D	5B	6F		
H	H	H	H	L	H	H	L	H		
H	L	H	H	H	L	H	H	L		
H	H	L	H	H	L	H	H	L		
H	L	L	L	H	L	H	H	L		

Table 4 : Logic Truth Table - Testing

T	P1	P2	3B	3C	5A	5C	5D	3D	5B	6F
L	H	H	L	L	H	L	H	L	L	H
L	L	H	H	L	H	L	H	L	L	H
L	H	L	L	H	H	L	H	L	L	H
L	L	L	H	H	L	H	L	L	H	L

The timer outputs are interfaced to their respective relays by 'open' collector transistors. The relays are arranged to stay de-energised if their supplies are interrupted and to require a manual reset.

4.0 Test Procedure

It is recommended that the monitor unit is tested before use, and every 1 to 2 months if in continual operation. This involves switching on the test, resetting the relays and checking that they both trip between 3 to 4 minutes after being reset.

5.0 Detailed Circuit Schematics & BOMs

Transmitter Monitor Schematic – trx_monitor.pdf
Transmitter Monitor Bill Of Materials – trx_monitor_BOM.xls
Probes & Test Circuit Schematic – probes.pdf
Probes & Test Circuit Bill Of Materials – probes_BOM.xls
Timers Schematic – timers.pdf
Timers Bill Of Materials – timers_BOM.xls

6.0 Failure Rate Analysis

Failure mode, effects and criticality analysis (FEMCA) is probably the most widely used and most effective design reliability analysis method. For electronic circuits the process involves examining the various failure modes of each component and determining whether they would result in a wrong side or right side failure. Failures are examined one at a time because it is expected that regular testing will uncover the fault before others could occur.

Note : A Wrong Side Failure (WSF) is one that could result in a dangerous state.
A Right Side Failure (RSF) is one that results in a safe outcome.

6.1 Power Supplies

The 230V 50 Hz to 12VDC power supply feeds the relays, the probe RF test oscillator and the 9VDC regulator for the timer board. The 9VDC regulator chip supplies both timers. Their failure modes are examined below because they can affect both time-out circuits:-

Table 4 : 12VDC PSU Failure Modes Analysis

Item	**Output Fault**	**Result**	**Outcome**
1	Voltage = 0	Relays de-energise removing power.	RSF
2	Voltage <50%	“ “ “ “	RSF
3	Voltage 50% - 90%	Timers time out early removing power.	RSF
4	Voltage 150% - 300%	9VDC regulator shuts down on over temperature de-energising the relays and removing power.	RSF
5	Voltage >300%	Not credible.	RSF

Table 5 : 9VDC Regulator Failure Modes Analysis

Item	Output Fault	Result	Outcome
1	Voltage = 0	Relays de-energise removing power.	RSF
2	Voltage 75% - 100%	Operation normal.	RSF
3	Voltage 30% - 70%	Timers speed up.	RSF
4	Voltage <30%	Relay K3 de-energised removing power due to insufficient drive to Q2.	RSF
5	Voltage 100% - 130%	May time out early due to more noise.	RSF
6	Voltage >130%	Not credible – limited by 12V source.	RSF

The rest of the monitor circuitry is divided between the two timers without any overlap in order to provide redundancy. Relatively few components were used and so in most cases the pessimistic assumption was made that any failure would be a Wrong Side Failure to simplify the analysis.

6.2 Timer Input Signals Failure Rates

The input signals to the two timers are derived in different ways as covered in the following sub-sections.

6.2.1 Timer 1

The transceiver relay part of the circuit is described in section 3.1. The wiring between this relay and the timer board is arranged so that any disconnection results in the loss of the reset signal and the timer-1 times out and trips the power (RSF). Note: The opto-isolator is treated as part of the timer board and its failure rate is taken into account there.

6.2.2 Timer 2

The probe circuit is described in section 3.2 and illustrated in Figure 2. The fully detailed schematic is given in probes.pdf and the associated document probes_BOM.xls.

The probe circuits are tested by injecting a 3.68MHz RF signal. Any failure in this signal injection would be revealed by the timer 2 circuit failing to pass its regular test (RSF).

The relays K1 & K2 are arranged so that any failure is a RSF.

Table 6 : Probes Failure Rate

Item	Component	Failure rate x (1.0E-6)	Total x (1.0E-6)	Source
1	R4 R5 R6 R7	4 x 0.084	0.0336	8.3
2	C4 C5 C6 C7	4 x 0.0077	0.0308	8.4
3	D1 D2	2 x 0.0014	0.0028	8.8
4	K1_base K2_base	2 x 0.056	0.112	8.13
5	P1S1 P2S2 P5S5 P6S6	4 x 0.00095	0.0038	8.14
		Summation =	0.183	

6.3 Timer Board Failure Rates

The timer board contains two independent timer circuits which are described in section 3.3 The detailed schematic is given in timers.pdf and the associated document timers_BOM.xls. The timers are supplied by the 9V regulator whose failure modes are shown in table 5 of section 6.1 to be all RSFs.

Table 7 : Timer Board Timer-1 Failure Rate

Item	**Component**	**Failure rate x (1.0E-6)**	**Total x (1.0E-6)**	**Source**
1	R1 R2 R5 R7 R8 R10 R12 R17	8 x 0.034	0.272	8.2
2	C1	1 x 0.0077	0.0077	8.6
3	D1	1 x 0.0014	0.0014	8.8
4	LED_D1	RSF	0.0	-
4	ZD1	1 x 0.043	0.043	8.9
5	Q1 Q2	2 x 0.0015	0.003	8.10
6	U1	1 x 0.45	0.45	8.11
7	U7	1 x 0.0082	0.0082	8.1
		Summation =	0.785	

Table 8 : Timer Board Timer-2 Failure rate

Item	**Component**	**Failure rate x (1.0E-6)**	**Total x (1.0E-6)**	**Source**
1	R3 R4 R6 R9 R11 R13	6 x 0.034	0.204	8.2
2	C2	1 x 0.0077	0.0077	8.6
3	D2	1 x 0.0014	0.0014	8.8
4	LED_D2	RSF	0.0	-
4	Q3	1 x 0.0015	0.0015	8.10
5	U2 U3	2 x 0.45	0.90	8.11
6	U4 U5 U6 U8	4 x 0.0082	0.0328	8.1
		Summation =	1.15	

Table 9 : Monitor – Timer-1 Overall Failure Rate

Item	Component	Failure rate x (1.0E-6)	Total x (1.0E-6)	Source
1	Probe assembly	Not applicable	0.0	-
2	Timer board Timer_1	1 x 0.785	0.785	Table 7
3	SW1	1 x 0.2	0.2	8.15
4	P5S5	RSF	0.0	-
5	K3	1 x 0.25	0.25	8.12
6	K3_base	RSF	0.0	8.14
		Summation =	**1.24**	

Table 10 : Monitor – Timer-2 Overall Failure Rate

Item	Component	Failure rate x (1.0E-6)	Total x (1.0E-6)	Source
1	Probe assembly	1 x 0.184	0.183	Table 6
2	Timer board Timer_2	1 x 0.785	1.15	Table 8
3	SW1	1 x 0.2	0.2	8.15
4	P5S5	RSF	0.0	-
5	K3	1 x 0.25	0.25	8.12
6	K3_base	RSF	0.0	8.14
		Summation =	**1.78**	

To summaries, the overall estimated failure rate for Timer-1 is 1.24E-6 failures per hour, and for timer-2 is 1.78E-6 failures per hour. This is well within the target figure of 10E-6 failures per hour for each timer. This leaves an allowance for soldering joint failures that were not quantified in the above tables.

6.3 Over Temperature Protection Failure Rate

It can be seen from the schematic diagram for the monitor (trx_monitor.pdf) that either thermostatic switch opening would remove the supply to the timer board. This in turn would de-energise the relays whose contacts supply the voltage to the transmitter equipment. The transmiter would therefore have its power removed unless both contacts on relay had a short circuit fault, and/or both bases had a short circuit. The following formulae can be found in Ref.6

The reliability of a component is calculated by :-

$$R = \exp(-t\lambda)$$

where R = Reliability (0 to 1)

t = Time at risk (hours)

λ = Failure rate (failures/hour)

The reliability of an arrangement where both components must fail for an overall failure is given by :-

$$R = 1 - (1 - R_1) \times (1 - R_2)$$

where R_1 & R_2 = The reliability of the two components

Hence the combined reliability of the thermostats is given by:-

$$Rtht = 1 - (1 - \exp(-t\lambda)) \times (1 - \exp(-t\lambda)) = 0.9999701$$

where t = 87600 hours (10 years)

λ = 0.062E-6 (see section 8.16)

Also the combined reliability of the pair of relays and bases is given by:-

$$Rrt = 1 - (1 - \exp(-t\lambda)) \times (1 - \exp(-t\lambda)) = 0.99999996$$

where t = 672 hours (tested every 4 weeks))

λ = 0.25E-6 + 0.056E-6 = 0.306E-6 (see sections 8.12 & 8.13)

The overall reliability is therefore given by:-

$$R_{overall} = Rtht \times Rrt = 0.9999700$$

This is equivalent to an overall failure rate calculated to be:-

$$\lambda_{equiv} = (\ln(R_{overall}))/ 87600 = 3.4E-10 \quad \text{(Target value 1.0E-9)}$$

To summaries, the overall liability is dominated by the failure rates of the thermostatic switches because they are untested over the design life of the monitor. Nevertheless the dual redundancy enables the target value of not more than one wrong side failure every 1000 000 000 hours to be met.

7.0 References

Ref.1 : License terms, conditions and limitations – Section 10, Remote operation - https://services.ofcom.org.uk/amateur-terms.pdf

Ref.2 : IEC 61508-1 : Functional safety of electrical/electronic/programmable electronic safety-related systems – Part 1, General requirements.

Ref.3 : hazop.pdf – http://g0vie.co.uk/ncradioclub/remote_op.html

Ref.4 : rel.interrsil.com/docs/rel/PEM/Mil_plas_11.html (cmos reliability figures)

Ref.5 : US MIL_HDBK_217 Rev.F, Notice 2 – Published 1995

Ref.6 : Practical reliability Engineering 3rd Edition, by P D T O'Connor, Pub. John Wiley & Sons.

8.0 Appendix A : Component Failure Rates

In the following, Ref.4 was used for the failure rates of the CMOS chips. All the other component failure rates were based on the data in US MIL Handbook in Ref.5 and scaled for commercial quality.

8.1 CMOS Chips

CD4011B, CD4020BEE4, HEF4060BP, CD4069BE :-
PDIP 8.2 FITS = 0.008.2 x 10E-6 failures per hour.

8.2 Metal Film Resistor, Fixed, 0.125W

$\lambda p = \lambda b \times \pi T \times \pi p \times \pi s \times \pi q \times \pi e \times$ 1.0E-6 Failures/hour

where λb = 0.0037 - Film, insulated
πT = 1.9 - 100°C case Temperature
πp = 0.44 - Power dissipation 0.13 Watts
πs = 1.1 - Power stress 0.4
πq = 10 - Commercial quality
πe = 1 - Ground based environment

∴ λp = 0.0037 x 1.9 x 0.44 x 1.1 x 10 x 1 x 10E-6 = 0.034 E-6

8.3 Metal Film Resistor, Fixed, 2W

$\lambda p = \lambda b \times \pi T \times \pi p \times \pi s \times \pi q \times \pi e \times$ 1.0E-6 Failures/hour

where λb = 0.0037 - Film, insulated
πT = 1.9 - 100°C case Temperature
πp = 1.0 - Power dissipation 1.0 Watts
πs = 1.2 - Power stress 0.5
πq = 10 - Commercial quality
πe = 1 - Ground based environment

∴ λp = 0.0037 x 1.9 x 1.0 x 1.2 x 10 x 1 x 10E-6 = 0.084 E-6

8.4 Capacitor, Fixed, Mica Dielectric

$\lambda p = \lambda b \times \pi T \times \pi c \times \pi v \times \pi q \times \pi e \times$ 1.0E-6 Failures/hour

where λb = 0.00076 - Film, insulated
πT = 2.9 - 50°C Ambient temperature
πc = 0.29 - < 0.000001μF

πv = 1.2 - Voltage stress 0.5
πq = 10 - Commercial quality
πe = 1 - Ground based environment

.'. λp = 0.00076 x 2.9 x 0.29 x 1.2 x 10 x 1 x 1.0E-6 = 0.0077 E-6

8.5 Capacitor, Fixed, Ceramic

λp = λb x πT x πc x πv x πq x πe x 10E-6 Failures/hour

where λb = 0.00099 - Ceramic, general purpose
πT = 2.9 - 50°C Ambient temperature
πc = 0.54 - < 0.001μF
πv = 1.0 - Voltage stress 0.2
πq = 10 - Commercial quality
πe = 1 - Ground based environment

.'. λp = 0.00099 x 2.9 x 0.54 x 1.0 x 10 x 1 x 1.0E-6 = 0.0155 E-6

8.6 Capacitor, Film, Polyester

λp = λb x πT x πc x πv x πq x πe x 10E-6 Failures/hour

where λb = 0.00051 - Metalised plastic
πT = 1.6 - 50°C Ambient temperature
πc = 0.94 - < 0.5μF
πv = 1.0 - Voltage stress 0.2
πq = 10 - Commercial quality
πe = 1 - Ground based environment

.'. λp = 0.00051 x 1.6 x 0.94 x 1.0 x 10 x 1 x 1.0E-6 = 0.0077 E-6

8.7 Capacitor, Fixed, Tantalum

λp = λb x πT x πc x πv x πrs x πq x πe x 10E-6 Failures/hour

where λb = 0.0004 - Tantalum, solid electrolyte
πT = 1.6 - 50°C Ambient temperature
πc = 2.3 - 47μF
πv = 2.0 - Voltage stress 0.5
πrs = 3.3 - R/V 0 – 0.1
πq = 10 - Commercial quality
πe = 1 - Ground based environment

'. λp = 0.0004 x 1.6 x 2.3 x 2.0 x 3.3 x 10 x 1 x 1.0E-6 = 0.097 E-6

8.8 Diode, Switching

$\lambda p = \lambda b \times \pi T \times \pi s \times \pi c \times \pi q \times \pi e \times$ 1.0E-6 Failures/hour

where λb = 0.001 - Low power, switching
πT = 5 - 80°C Junction temperature
πs = 0.054 - Voltage stress < 0.3
πc = 1 - Bonded construction
πq = 5 - Commercial quality
πe = 1 - Ground based environment

∴ λp = 0.001 x 5 x 0.054 x 1 x 5 x 1 x 1.0E-6 = 0.0014 E-6

8.9 Zener Diode

$\lambda p = \lambda b \times \pi T \times \pi s \times \pi c \times \pi q \times \pi e \times$ 1.0E-6 Failures/hour

where λb = 0.002 - Low power, switching
πT = 2.7 - 80°C Junction temperature
πs = 1 - Voltage regulator
πc = 1 - Bonded construction
πq = 8 - Plastic
πe = 1 - Ground based environment

∴ λp = 0.002 x 2.7 x 1 x 1 x 8 x 1 x 1.0E-6 = 0.043 E-6

8.10 Bipolar Transistor

$\lambda p = \lambda b \times \pi T \times \pi a \times \pi r \times \pi s \times \pi q \times \pi e \times$ 1.0E-6 Failures/hour

where λb = 0.00074 - bipolar, Frequency <200MHz
πT = 4.2 - 800°C Junction temperature
πa = 0.7 - Application, switching
πr = 0.77 - Power 0.5W
πs = 0.11 - V/Rated 0.3
πq = 8 - Commercial, plastic
πe = 1 - Ground based environment

∴ λp = 0.00074 x 4.2 x 0.7 x 0.77 x 0.11 x 8 x 1 x 1.0E-6 = 0.0015 E-6

8.11 Opto-isolator

$\lambda p = \lambda b \times \pi T \times \pi q \times \pi e \times 1.0E\text{-}6$ Failures/hour

where	λb	=	0.013	- phototransistor
	πT	=	4.3	- 80°C Junction temperature
	πq	=	8	- Commercial, plastic
	πe	=	1	- Ground based environment

∴ $\lambda p = 0.013 \times 4.3 \times 8 \times 1 \times 1.0E\text{-}6 = 0.45\ E\text{-}6$

8.12 Relay DPDT

$\lambda p = \lambda b \times \pi L \times \pi c \times \pi cyc \times \pi f \times \pi q \times \pi e \times 1.0E\text{-}6$ Failures/hour

where	λb	=	0.013	- 60°C Ambient, Rated 85°C
	πL	=	1.48	- Load Stress 0.5
	πc	=	1.5	- DPST – Active contacts
	πcyc	=	1.0	- <10 cycles per hour
	πf	=	3	- General purpose, armature
	πq	=	2.9	- Commercial
	πe	=	1	- Ground based environment

∴ $\lambda p = 0.013 \times 1.48 \times 1.5 \times 1.0 \times 3 \times 2.9\ 1 \times 1.0E\text{-}6 = 0.25\ E\text{-}6$

8.13 Relay Base

$\lambda p = \lambda b \times \pi p \times \pi q \times \pi e \times 1.0E\text{-}6$ Failures/hour

where	λb	=	0.037	- Single line
	πp	=	1.5	- 2 Active pins
	πq	=	1.0	- Lower
	πe	=	1	- Ground based environment

∴ $\lambda p = 0.037 \times 1.5 \times 1 \times 1.0E\text{-}6 = 0.056$

8.14 PCB Connector 2-Pin

$\lambda p = \lambda b \times \pi p \times \pi q \times \pi e \times 1.0E\text{-}6$ Failures/hour

where	λb	=	0.00064	- Single line
	πp	=	1.5	- 2 Active pins
	πq	=	1.0	- Lower
	πe	=	1	- Ground based environment

∴ $\lambda p = 0.00064 \times 1.5 \times 1 \times 1.0E\text{-}6 = 0.00096\ E\text{-}6$

8.15 Push Button Switch

$\lambda p = \lambda b \times \pi L \times \pi c \times \pi q \times \pi e \times$ 1.0E-6 Failures/hour

where	λb	=	0.1	- Push button switch
	πL	=	1.0	- Load stress 0.05
	πc	=	1.0	- SPST
	πq	=	2.0	- Lower
	πe	=	1	- Ground based environment

.'. λp = 0.1 x 1.0 x 1.0 x 2.0 x 1 x 1.0E-6 = 0.2 E-6

8.16 Thermostatic Switch

$\lambda p = \lambda b \times \pi L \times \pi c \times \pi q \times \pi e \times$ 1.0E-6 Failures/hour

where	λb	=	0.031	- Thermal switch
	πL	=	1.0	- Load stress 0.05
	πc	=	1.0	- SPST
	πq	=	2.0	- Lower
	πe	=	1	- Ground based environment

.'. λp = 0.031 x 1.0 x 1.0 x 2.0 x 1 x 1.0E-6 = 0.062 E-6

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